VLSI Design *Distance Learning*

Course Part# PCBkeyVLSI0213

CEDA
www.ceda.in
Centre for Electronics Design and Automation

Learning Objectives

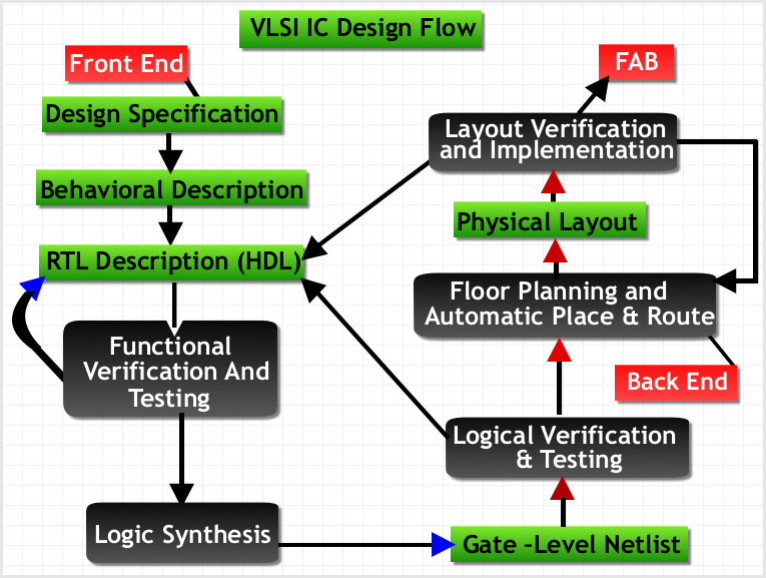
Learn the skills you need to succeed as a VLSI design engineer - at home, at your own pace. Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip.

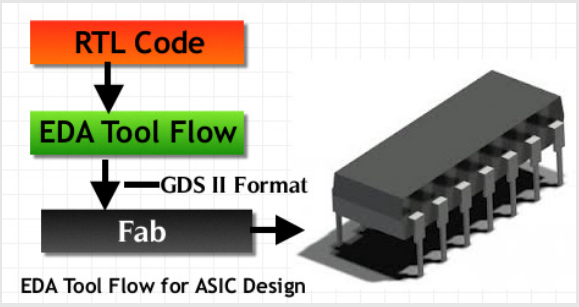
This training is based on FPGA design flow with Xilinx tools. This program will help you to design Complex digital systems using Verilog and also to get experience of Processor and controller implementations on FPGAs.

Training modules start with solid basics. You'll begin by learning the important principles that are the fundamental rules for just about whatever you may do in VLSI design. Then, you'll get detailed instruction in techniques and procedures. Step by step, we'll guide you through exciting hands-on projects like Processor implementation on FPGA that you can complete in your PC anywhere

Courseware Includes

- Audio-Video Session in USB Pen drive
- VLSI Board – Xilinx Spartan based
- USB Cable JTAG with Parallel Cable
- ModelSIM Timing Simulation Software
- Xilinx ISE Software
- Verilog Example codes
- User Manual Hard copy
- VLSI Board Schematics, Data Sheet
- Reference Book





EDA Tool Flow for ASIC Design

Board Features:
- 100,000 gate Xilinx Spartan 3E FPGA
- JTAG programming port
- XCF04S Xilinx Platform Flash ROM to store FPGA configurations
- Large collection of I/Os including eight LED's and four slide switches
- LCD and 7 segment displays
- RS 232 and VGA ports
- Ethernet port with physical layer controller
- User-selectable oscillator, plus a socket for a second oscillator
- 100 pin user I/O and peripheral module connection

FPGA Features:
- 100k gates.
- 108 I/Os.
- 72k Block RAM.
- 15k Distributed RAM.
- 240 CLBs.

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***Learning Objectives** Audio-Video Sessions*

1. Introduction to VLSI design
• VLSI definition
• Why VLSI needed
• What is a Silicon chip
• Silicon Die and Layout
• Classification of Chip based on Fabrication
• Process technologies
• Chip manufacturing processes
• MOS technology trends
• VLSI products
• Scope of VLSI – different Domains and Fields
• Challenges and trends – power, speed and area

2. Basic Digital Design
• Arithmetic circuits
Half Adder & Full Adder
Binary Adder /Subtracter & Multiplier

• Sequential and Combinational circuits
a) Encoder and Decoder
b) Multiplexer and De multiplexer
c) Flip-Flop and Latches
d) D ff, JK ff, T ff
e) Registers and Counters

• State machines
State diagram, Mealy Moore machine

Digital design issues
a) Met stability
b) Setup and Hold Time c) Clock skew3.

Verilog HDL- 1995 and 2001 Verilog
• Introduction to HDL
• Different HDL comparison VHDL, Verilog, System Verilog, System C
• Verilog Program structure
• Different Style of modeling
a) Structural style
b) Data Flow style
c) Behavioral style• Data types
a) Net type b) Reg type

• Operators
• Compiler directives
• Blocking and Non Blocking Statements
• User Defined Primitives
• Timing Control Statements
a) Delay
b) Event control
c) Wait
Conditional Statements
a) if and if – else statement
b) case statement

• Looping Statements
a) for loop, while loop , forever loop, repeat

• Functions and Task
a) User functions and tasks
b) System tasks

• Memory modeling
RAM & ROM modeling

• Reset modeling
a) Synchronous Modeling
b) Asynchronous Modeling

• Test bench modeling
a) Mux Modeling and testing
b) Counter modeling and testing

• 2001 Verilog features
a) Combined port and data type
b) ANSI style of port declarations
c) Combinational sensitivity token
d) Comma separator for sensitivity list
e) Power Operator
f) Signed Data types
g) Multidimensional array
• Generate Loop

4. How to Use Modelsim for Design HDL and Simulation
• Basic designs modeling using Modelsim- Basic gates and Counter
• Compiling the design
• Simulation of Design using Modelsim
a) Assigning inputs and clock
b) Generate wave form and collect the output

5. Programmable devices
• CPLD, FPGAs, more about Xilinx FPGAs
• Programmable Logic and technologies
• PLA and PAL
• CPLD Architecture
• FPGA Architecture
• Xilinx FPGA architecture, Xilinx Spartan FPGA

6. FPGA Design Flow
• Steps in Design Flow
• Device Programming
• Xilinx FPGA programming through JTAG

7. How to make and implement a Design Using Xilinx ISE
• Basic HDL coding
• Basic gates, Flip Flop and counter
• Verilog HDL synthesis
a) Basic gates, Flip Flop and counter lease ask for the quotation

• Implement the design and generate bit file
a) Basic gates, Flip Flop and counter

• Generate PROM file
a) Download the configuration file in to FPGA using xilinx Impact Connect JTAG cable Initialize JTAG chain and detect FPGA part number Program the FPGA

8. Implementation of 8 bit Picoblaze Processor in Xilinx FPGA
• Study of Picoblaze processor architecture
• Features and Instruction set of Picoblaze